

DATA SHEET

SC26C562

CMOS dual universal serial
communications controller (CDUSCC)

Product specification
Supersedes data of 1995 May 01
IC19 Data Handbook

1998 Sep 04

CMOS dual universal serial communications controller (CDUSCC)

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DESCRIPTION

The Philips Semiconductors SC26C562 Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC26C562 interfaces to synchronous bus MPUs and is capable of program-pollled, interrupt driven, block-move or DMA data transfers.

The SC26C562 (CDUSCC) is (PIN) hardware and (REGISTER) software compatible with the existing SC26C562 (DUSCC). CDUSCC will automatically configure to the NMOS DUSCC register map (default mode) on power up.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the CDUSCC well-suited for dual-speed channel applications. Data rates up to 10Mbits per second are supported.

The transmitter and receiver each contain a sixteen-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to sixteen characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

The SC26C562 CDUSCC is optimized to interface with processors using a synchronous bus interface, such as the 8086, and iAPX86 family. For systems using an asynchronous bus, such as the 68000 and 68010, refer to the SC68C562 documentation.

Refer to the CMOS Dual Universal Serial Communication Controller (CDUSCC) User's Manual for a complete operational description.

FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multi-protocol operation
 - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
 - COP: Single SYNC, dual SYNC, BiSYNC, DDCMP
 - ASYNC: 5-8 bits plus optional parity
- Sixteen character receive and transmit FIFOs with interrupt threshold control
- FIFO'ed status bits
- Watchdog timer
- 0 to 10 Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
 - 19 fixed rates: 50 to 64K baud
 - One user-defined rate derived from programmable counter/timer
 - External 1X or 16X clock
 - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- or half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
 - Compatible with Synchronous and Asynchronous bus DMA controllers
 - Half- or full-duplex operation
 - Single or dual address data transfers
 - Automatic frame termination on counter/ timer terminal count or DMA DONE (EOPN)
- Transmit path clear status
- High speed data bus interface: 160ns bus cycle
- DPLL operation up to 312.5kHz with internal clock
- Interrupt capabilities
 - Vector output (fixed or modified by status)
 - Individual interrupt enable bits
 - Programmable internal priorities
 - Maskable interrupt conditions
 - 80XX/X compatible
- Multi-function programmable 16-bit counter/timer
 - Bit rate generator
 - Event counter
 - Count received or transmitted characters
 - Delay generator
 - Automatic bit length measurement
- Modem controls
 - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
 - CTS and DCD programmable auto-enables for Tx and Rx
 - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits

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- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun and framing error detection
- False start bit detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit and receive up to 10Mbps at 1x or 1Mbps at 16x data rates

Bit-Oriented Protocol

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Transmit 7 or 8 bit ABORT
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields

- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

Character-Oriented Protocols

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill or underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun and underrun error detection
- Optional SYNC exclusion from FCS
- BISYNC features
 - EBCDIC or ASCII header, text and control messages
 - SYN, DLE stripping
 - EOM (end of message) detection and transmission
 - Auto transparency mode switching
 - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
 - Control character sequence detection for both transparent and normal text
 - Parity generation for data and LRC characters

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL	INDUSTRIAL	DWG #
	Serial Data Rate = 10Mbps Maximum	Serial Data Rate = 8Mbps Maximum	
48-Pin Plastic Dual In-Line Package (DIP)	SC26C562C1N	Not available	SOT240-1
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SC26C562C1A	SC26C562A8A	SOT238-3

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATING		UNIT
		COMMERCIAL	INDUSTRIAL	
T _A	Operating ambient temperature ²	0 to +70	-40 to +85	°C
T _{STG}	Storage temperature	-65 to +150	-65 to +150	°C
V _{CC}	Voltage from V _{CC} to GND ³	-0.5 to +7.0	-0.5 to +7.0	V
V _S	Voltage from any pin to ground ³	-0.5 to V _{CC} +0.5	-0.5 to V _{CC} +0.5	V

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PIN CONFIGURATIONS

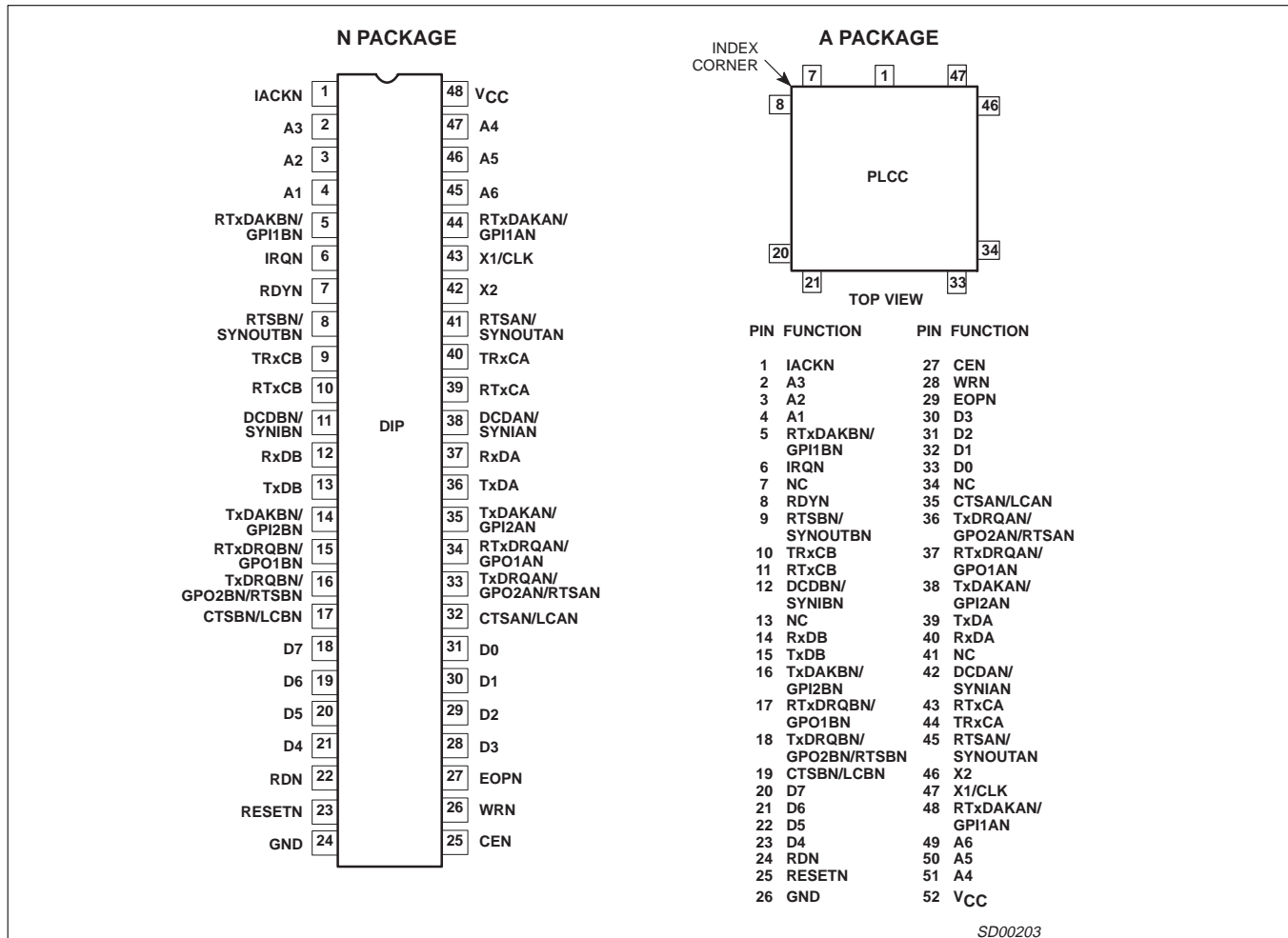


Figure 1. Pin Configurations

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BLOCK DIAGRAM

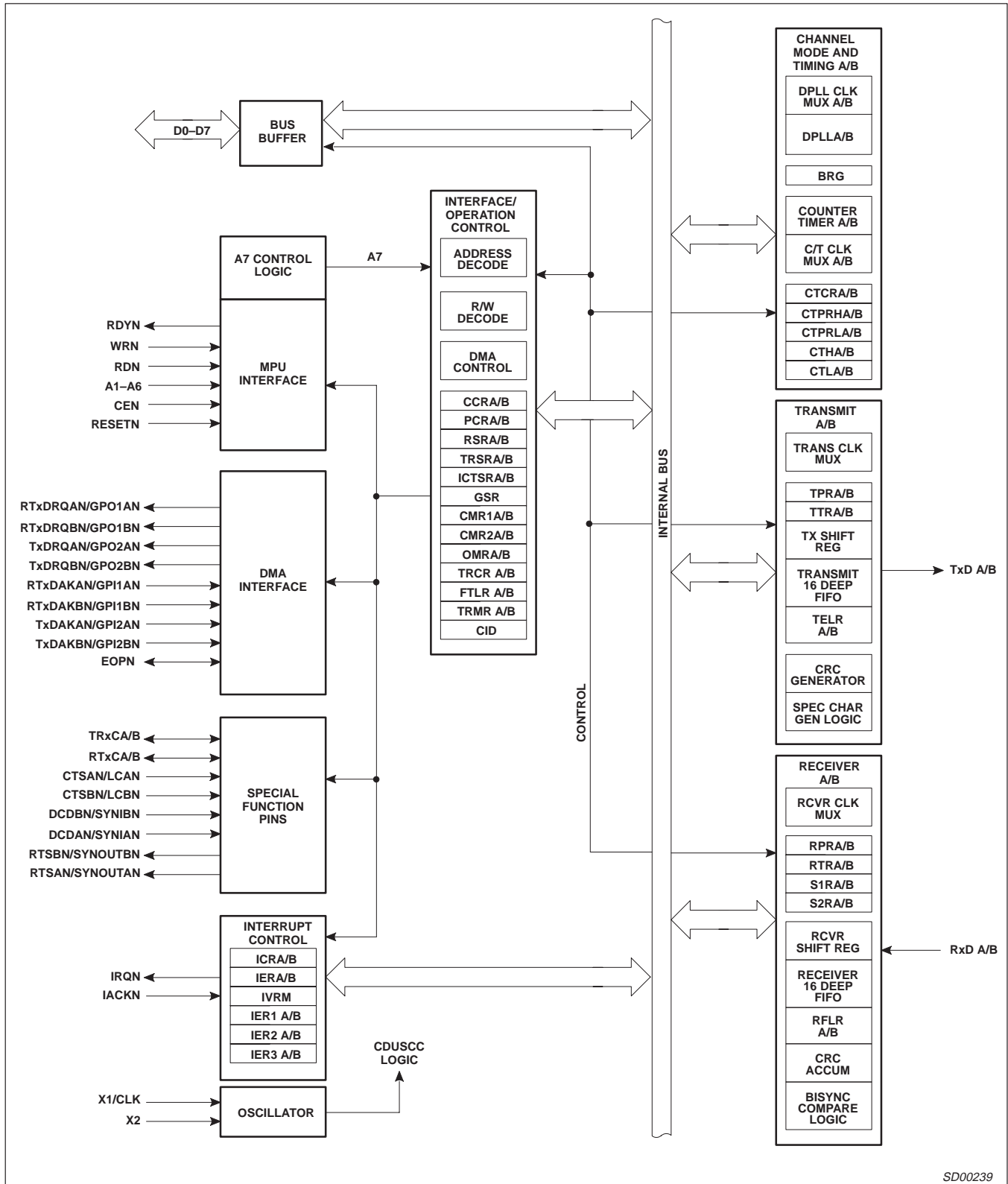


Figure 2. Block Diagram

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PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4-2, 47-45	4-2, 51-49	I	Address Lines: Active-high. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	31-28, 21-18	33-30, 23-20	I/O	Bidirectional Data Bus: Active-high, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the CDUSCC take place over this bus. The data bus is enabled when CSN and RDN, or CSN and WRRN are low during interrupt acknowledge cycles and single address DMA acknowledge cycles.
RDN	22	24	I	Read Strobe: Active-low input. When active and CSN is also active, causes the content of the addressed register to be present on the data bus. RDN is ignored unless CSN is active.
WRN	26	28	I	Write Strobe: Active-low input. When active and CSN is also active, the content of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of WRN. WRN is ignored unless CEN is active.
CSN	25	27	I	Chip Select: Active-low input. When active, data transfers between the CPU and the CDUSCC are enabled on D0–D7 as controlled by RDN or WRN and A1–A6 inputs. When CSN is high, the data lines are placed in the 3-State condition (except during interrupt acknowledge cycles and single address DMA transfers).
RDYN	7	8	O	Ready: Active-low, open drain. Used to synchronize data transfers between the CPU and the CDUSCC. It is valid only during read and write cycles where the CDUSCC is configured in 'wait on Rx', 'wait on Tx' or 'wait on Tx or Rx' modes, otherwise it is always inactive. RDYN becomes active on the leading edge of RDN and WRN if the requested operation cannot be performed (viz, no data in RxFIFO in the case of a read or no room in the TxFIFO in the case of a write).
IRQN	6	6	O	Interrupt Request: Active-low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the CDUSCC to output an interrupt vector on the data bus.
IACKN	1	1	I	Interrupt Acknowledge: Active-low. When IACKN is asserted, the CDUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	43	47	I	Crystal or External Clock: When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.
X2	42	46	O	Crystal 2: Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground. If an external clock is used on X1, this pin should be left floating.
RESETN	23	25	I	Master Reset: Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	40, 14	I	Channel A (B) Receiver Serial Data Input: The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	39, 15	O	Channel A (B) Transmitter Serial Data Output: The least significant bit is transmitted first. This output is in the marking (high) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	43, 11	I/O	Channel A (B) Receiver/Transmitter Clock: As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	40, 9	44, 10	I/O	Channel A (B) Transmitter/Receiver Clock: As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1 ÷ 2).

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PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	Channel A (B) Clear-to-Send Input or Loop Control Output: Active-low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The CDUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by CDUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	Channel A (B) Data Carrier Detected or External Sync Input: The function of this pin is programmable. As a DCD active-low input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the CDUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-low external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output: Active-low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send: Active-low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input: Active-low. For half-duplex single address operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	Channel A (B) Transmitter DMA Acknowledge or General Purpose Input: Active-low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the CDUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
EOPN	27	29	I/O	Done (EOP): Active-low, open-drain. EOPN can be used and is active in both DMA and non-DMA modes. As an input, EOPN indicates the last DMA transfer cycle to the Tx FIFO. As an output, EOPN indicates either the last DMA transfer from the Rx FIFO or that the transmitted character count has reached terminal count.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	Channel A (B) Sync Detect or Request-to-Send: Active-low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V _{CC}	48	34, 52	I	+5V Power Input
GND	24	26, 13, 41, 7	I	Signal and Power Ground Input

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DC ELECTRICAL CHARACTERISTICS^{4,5} $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$ ^{4,5}

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage: All except X1/CLK				0.8	V
V_{IH}	Input high voltage except X1/CLK	0 to 70°C	2.0		0.8	V
	X1/CLK	-40 to $+85^\circ\text{C}$	2.3			V
			$0.8 \times V_{CC}$		V_{CC}	V
V_{OL}	Output low voltage: All except IRQN ⁷	$I_{OL} = 5.3\text{mA (Comm)}, 4.8\text{mA (Ind)}$			0.5	V
V_{OH}	Output high voltage: (Except open drain outputs)	$I_{OL} = 8.8\text{mA (Comm)}, 7.8\text{mA (Ind)}$ $I_{OH} = -400\mu\text{A}$	$V_{CC} - 0.5$		0.5	V
I_{ILX1}	X1/CLK input low current ¹⁰	$V_{IN} = 0$, X2 = open			0.0	μA
I_{IHx1}	X1/CLK input high current ¹⁰	$V_{IN} = V_{CC}$, X2 = GND	-150		150	μA
I_{SCX2}	X2 short circuit current	X1 = open, $V_{IN} = 0$ $V_{IN} = V_{CC}$			-15 +15	mA mA
I_{IL}	Input low current RESETN, TxDAKN, RxDAKN	$V_{IN} = 0$	-15		-0.5	μA
I_I	Input leakage current	$V_{IN} = 0$ to V_{CC} , 0 to 70°C -40 to $+85^\circ\text{C}$	-1 -10		+1 +10	μA
I_{OZH}	Output off current high, 3-State data bus	$V_{IN} = V_{CC}$, 0 to 70°C -40 to $+85^\circ\text{C}$			+1 +10	μA
I_{OZL}	Output off current low, 3-State data bus	$V_{IN} = 0$, 0 to 70°C -40 to $+85^\circ\text{C}$	-1 -10			μA
I_{ODL}	Open drain output low current in off state: EOPN, RDYN	$V_{IN} = 0$	-15 -1		-0.5	μA μA
I_{ODH}	Open drain output high current in off state: EOPN, IRQN, RDYN	$V_{IN} = V_{CC}$	-1		1	μA
I_{CC}^{13}	Power supply current (see Figure 19 for graphs)	0 to 70°C -40 to $+85^\circ\text{C}$		25	80 95	mA
C_{IN}	Input capacitance ⁹	$V_{CC} = \text{GND} = 0$			10	pF
C_{OUT}	Output capacitance ⁹	$V_{CC} = \text{GND} = 0$			15	pF
$C_{I/O}$	Input/output capacitance ⁹	$V_{CC} = \text{GND} = 0$			20	pF

NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
- Clock may be stopped (DC) for testing purposes, or when CDUSCC is in non-operational modes.
- This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
- Parameters are valid over specified temperature range.
- All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.2V and 3.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.2V and 4.4V. All time measurements are referenced at input voltages of 0.2V and 3.0V and output voltages of 0.8V and 2.0V, as appropriate.
- See Figure 20 for test conditions for outputs.
- Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures true switching has occurred.
- Execution of the valid command (after it is latched) requires 3 rising edges of X1 (see Figure 15).
- These values were not explicitly tested; they are guaranteed by design and characterization data.
- X1/CLK and X2 are not tested with a crystal installed.
- X1/CLK frequency must be at least the faster of the receiver or transmitter serial data rate.
- Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CSN as the 'strobing' input. CSN and RDN (also CSN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
- $V_O = 0$ to V_{CC} , Rx and Tx clocks at 10MHz, X1 clock at 10MHz.

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AC ELECTRICAL CHARACTERISTICS^{4,5,6,7} $T_A = 0^\circ\text{C to } +70^\circ\text{C, } -40 \text{ to } +85^\circ\text{C, } V_{CC} = 5\text{V } \pm 10\%$

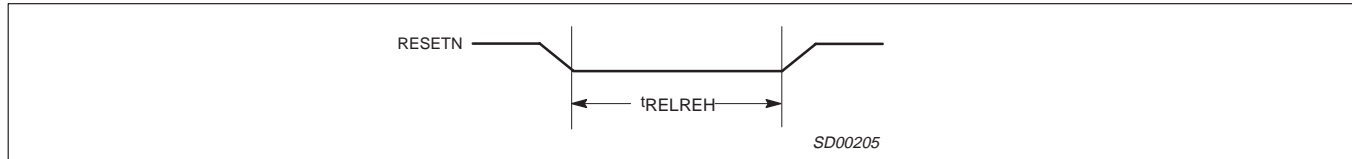


Figure 3. Reset Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{RELREH}	RESETN low to RESETN high	200		200		ns

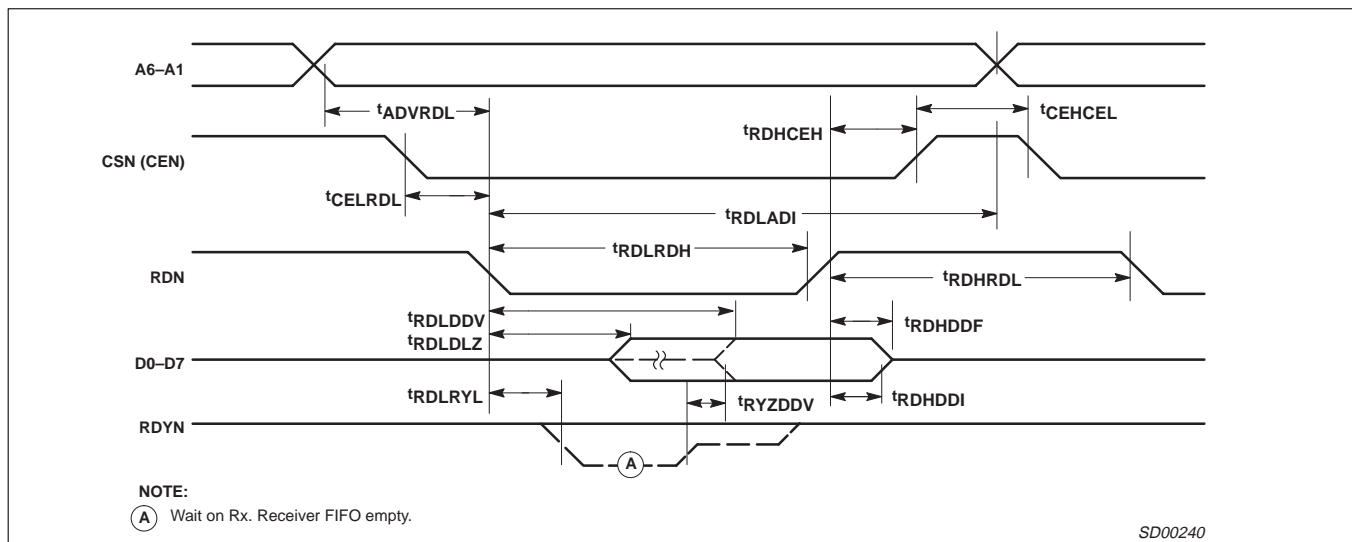


Figure 4. Read Cycle¹²

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{ADVRDL}	Address valid to RDN low	10		5		ns
t_{CELRLD}	CEN low to RDN low	10		0		ns
t_{RDLADI}	RDN low to address invalid	60		50		ns
t_{RDRLYL}	RDN low to RDYN low		160		150	ns
t_{RDLDLV}	RDN low to read data valid		150		130	ns
t_{RDLRDH}	RDN low to RDN high	150		130		ns
t_{RYZDDV}	RDYN high impedance to read data valid ⁹		90		90	ns
t_{RDHCEH}	RDN high to CEN high	10		0		ns
t_{CEHCEL}	CEN high to CEN low	50		30		ns
t_{RDHDDI}	RDN high to read data invalid	5		5		ns
t_{RDHRDL}	RDN high to RDN low	50		30		ns
t_{RDHDDF}	RDN high to data bus floating		50		40	ns
t_{RDLDLZ}	RDN low to data bus low impedance ⁹	5		10		ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

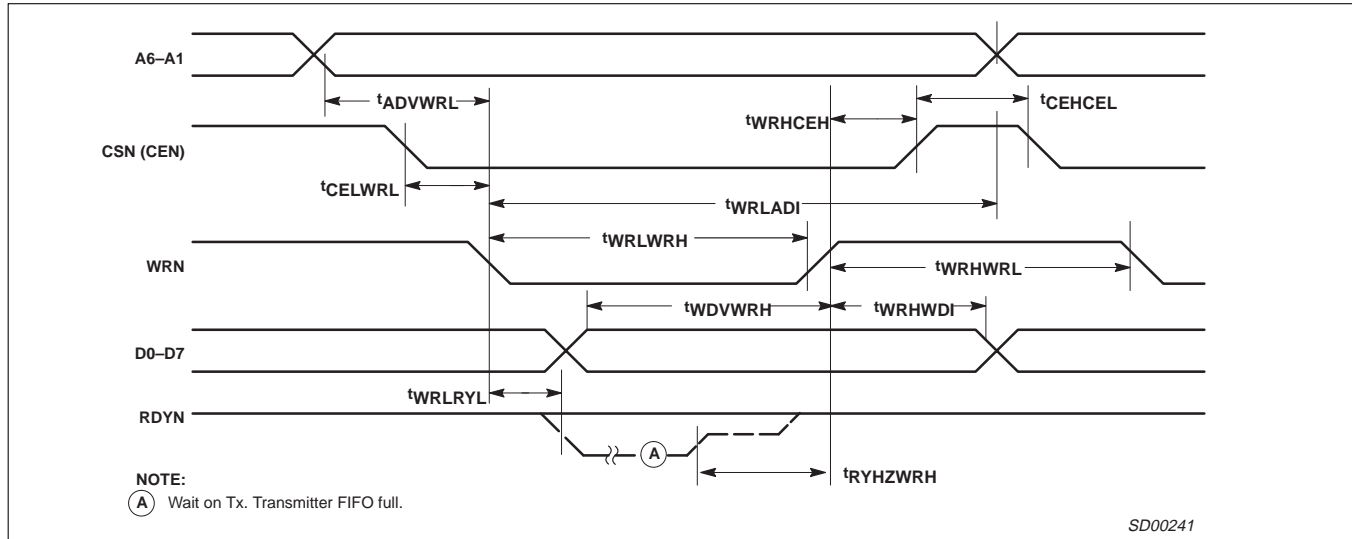


Figure 5. Write Cycle¹²

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{ADVWRL}	Address valid to WRN low	10		5		ns
t_{CEHWRL}	CSN low to WRN low	10		0		ns
t_{WRLRYL}	WRN low to RDYN low					ns
t_{WRHCEH}	WRN high to CSN high	10		0		ns
t_{WRLWRH}	WRN low to WRN high	110		100		ns
t_{WDVWRH}	Write data valid to WRN high	65		60		ns
t_{CEHCEL}	CEN high to CEN low	50	160	30	150	ns
t_{WRLADI}	WRN low to address invalid	60		50		ns
t_{WRHWRL}	WRN high to WRN low	50		30		ns
t_{WRHWDI}	WRN high to write data invalid	10		5		ns
$t_{RYHZWRH}$	RDYN hi impedance to WRN high ⁹	10		0		ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

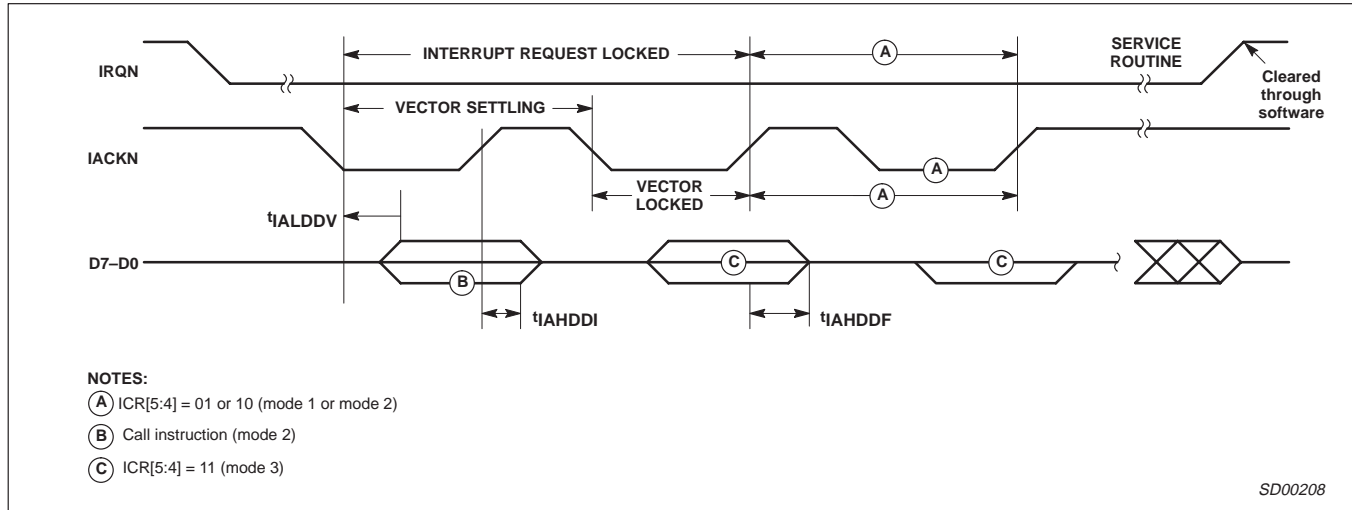


Figure 6. Interrupt Acknowledge Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{IALDDV}	IACKN low to data bus valid					ns
t_{IAHDDF}	IACKN high to data bus floating		140		130	ns
t_{IAHDDI}	IACKN high to data bus invalid	5	60	5	60	ns
t_{IALDLZ}	IACKN low to data bus low impedance ⁹	5		10		ns
t_{IAHIAL}	IACKN high to low	40		30		ns

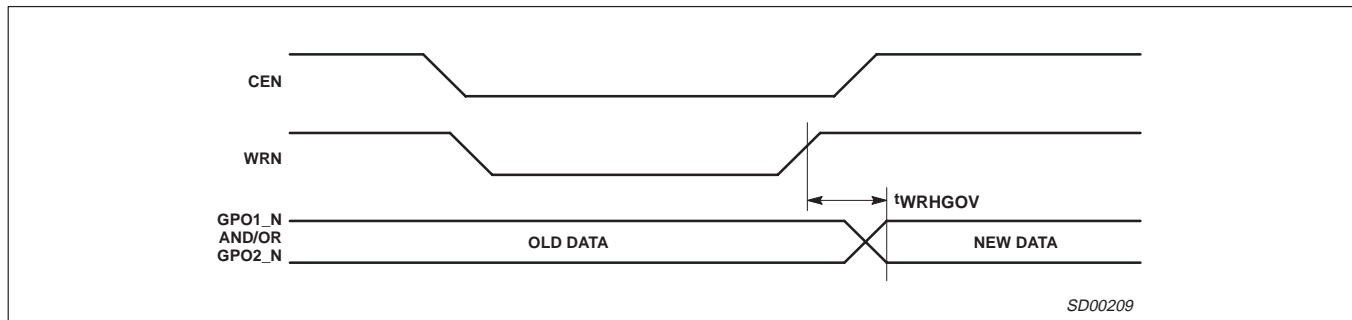


Figure 7. Output Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{WRHGOV}	WRN high to GPO output data valid		100		100	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

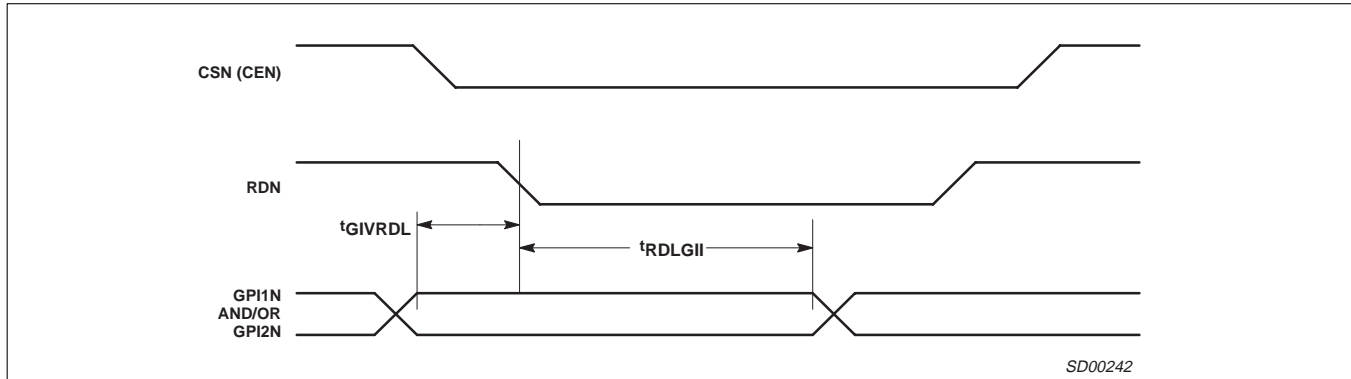


Figure 8. Input Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{GIVRDL}	GPI input valid to RDN low	20		20		ns
t_{RDLGII}	RDN low to GPI input invalid	40		40		ns

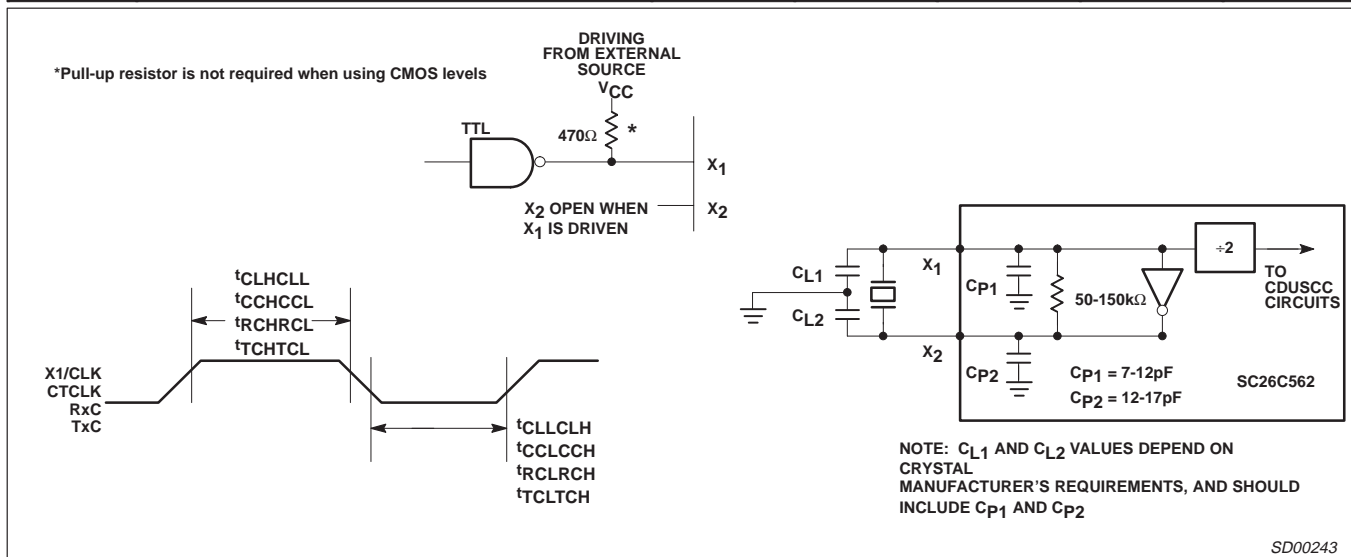


Figure 9. Clock Timing

SYMBOL	PARAMETER	LIMITS						UNIT
		INDUSTRIAL SC26C562			COMMERCIAL SC26C562			
		Min	Typ	Max	Min	Typ	Max	
t_{CLHCLL}	X1/CLK high to low time	25			25			ns
t_{CLLCLH}	X1/CLK low to high time	25			25			ns
t_{CCHCCL}	C/T CLK high to low time	50			45			ns
t_{CCLCCH}	C/T CLK low to high time	50			45			ns
t_{RCHRCL}	RxC high to low time	55			50			ns
t_{RCLRCH}	RxC low to high time	55			50			ns
t_{TCHTCL}	TxC high to low time	55			50			ns
t_{TCLTCH}	TxC low to high time	55			50			ns
f_{CL}	X1/CLK frequency ¹¹	0		16.0	0		16.0	MHz
f_{CC}	C/T CLK frequency	0	14.7456	8	0	14.7456	10	MHz
f_{RC}	RxC frequency (16X or 1X @ 50% duty cycle)	0		8	0		10	MHz
f_{TC}	TxC frequency (16X or 1X @ 50% duty cycle)	0		8	0		10	MHz
f_{RTC}	Tx/Rx frequency for FM/Manchester encoding			4			5	MHz

CMOS dual universal serial communications controller (CDUSCC)

SC26C562

AC ELECTRICAL CHARACTERISTICS (Continued)

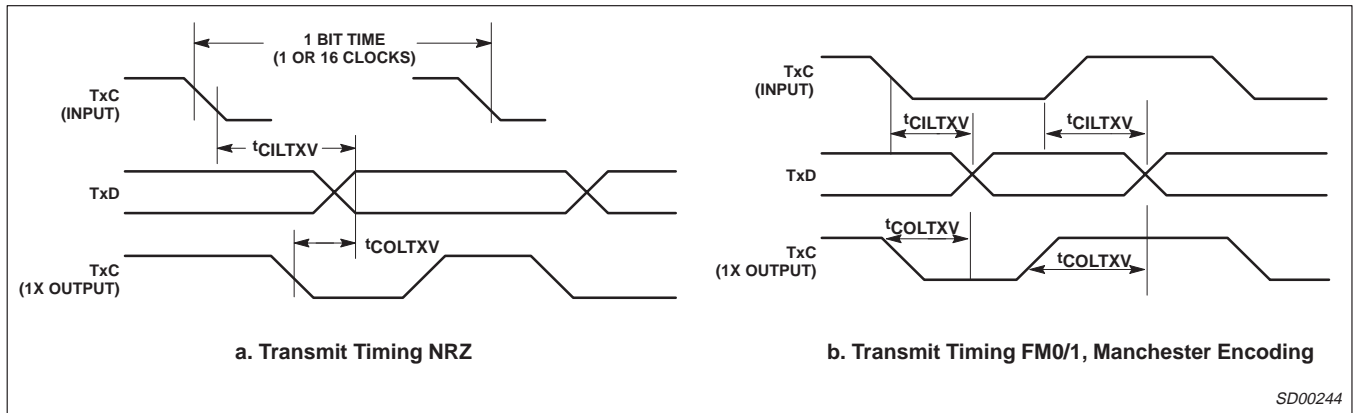


Figure 10.

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{CILTXV}	TxC input low (1X) to TxD output TxC input low (16X) to TxD output		120		120	ns
t_{COLTXV}^*	TxC output low to TxD output ⁹ (NRZ, NRZI) FM, MAN		25 35		20 30	ns

*Characterized with no loads on TxD and TxC outputs. Tester load is approximately 50pF.

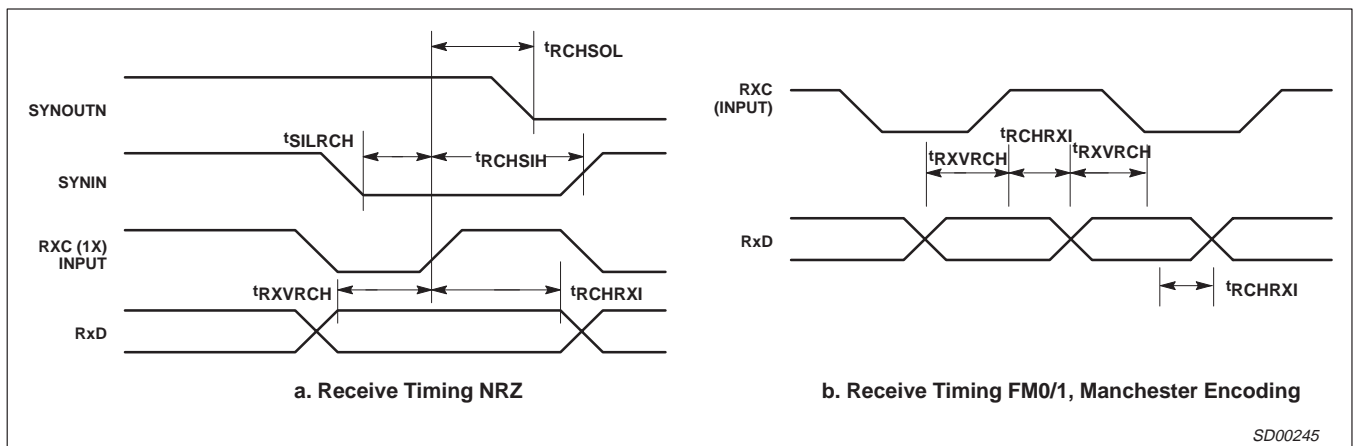


Figure 11.

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{RXVRCH}	RxD data valid to RxC high: For NRZ data For NRZI, Manchester, FM0, FM1 data	25 30		20 30		ns
t_{RCHRXI}	RxC high to RxD data invalid: For NRZ data For NRZI, Manchester, FM0, FM1 data	25 30		20 30		ns
t_{SILRCH}	SYNIN low to RxC high	50		50		ns
t_{RCHSIH}	RxC high to SYNIN high	20		20		ns
t_{RCHSOL}	RxC high to SYNOUT low		110		100	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

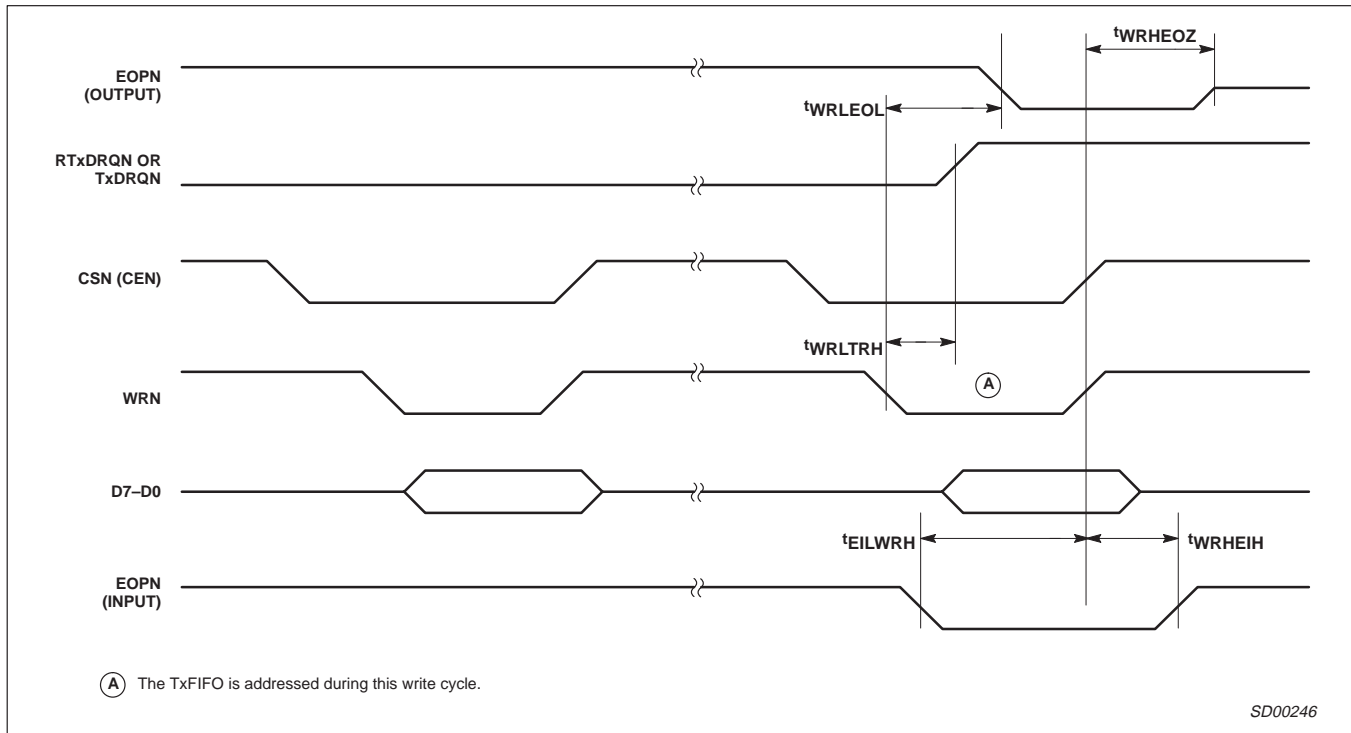


Figure 12. Transmit Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t _{WRLTRH}	WRN low to Tx DMA REQN high					ns
t _{WRLEOL}	WRN low to EOPN output low		110		100	ns
t _{WRHEOZ}	WRN high to EOPN output high impedance		110		100	ns
t _{EILWRH}	EOPN input low to WRN high	35	70	30	60	ns
t _{WRHEIH}	WRN high to EOPN input high	30		25		ns

CMOS dual universal serial communications controller (CDUSCC)

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AC ELECTRICAL CHARACTERISTICS (Continued)

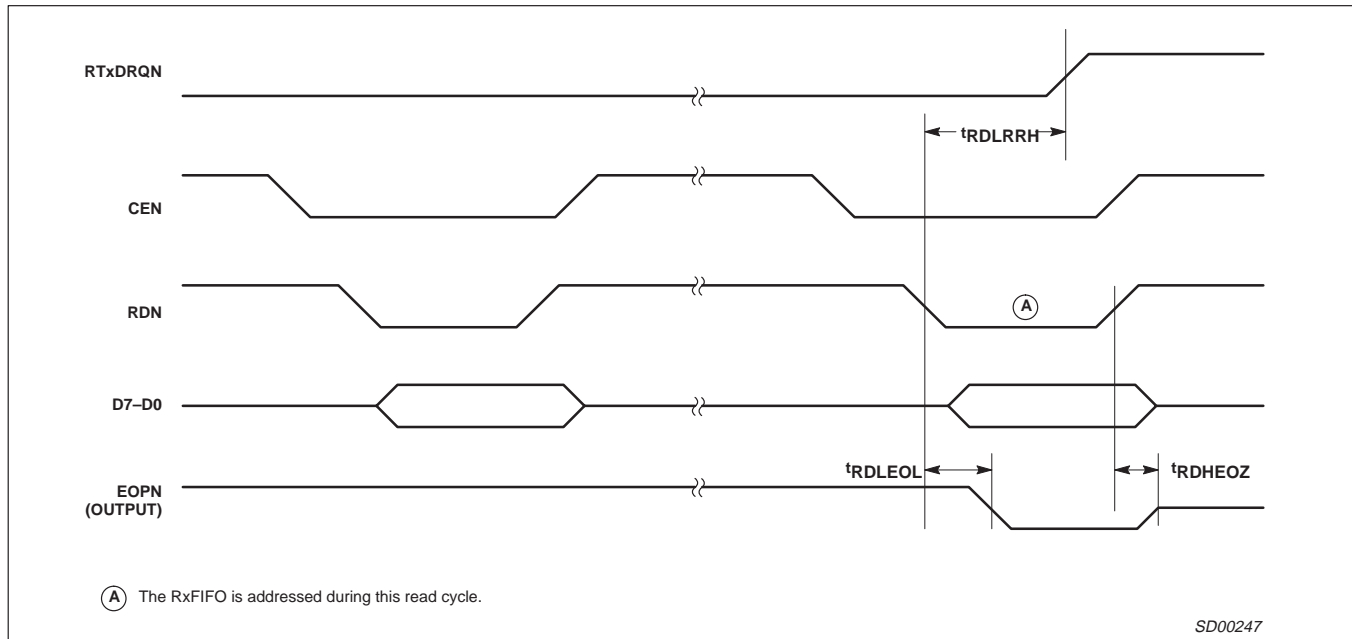


Figure 13. Receive Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t _{RDLEOL}	RDN low to Rx DMA REQN high		110		100	ns
t _{RDLEOL}	RDN low to EOPN output low		110		100	ns
t _{RDHEOZ}	RDN high to EOPN output high impedance		70		60	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

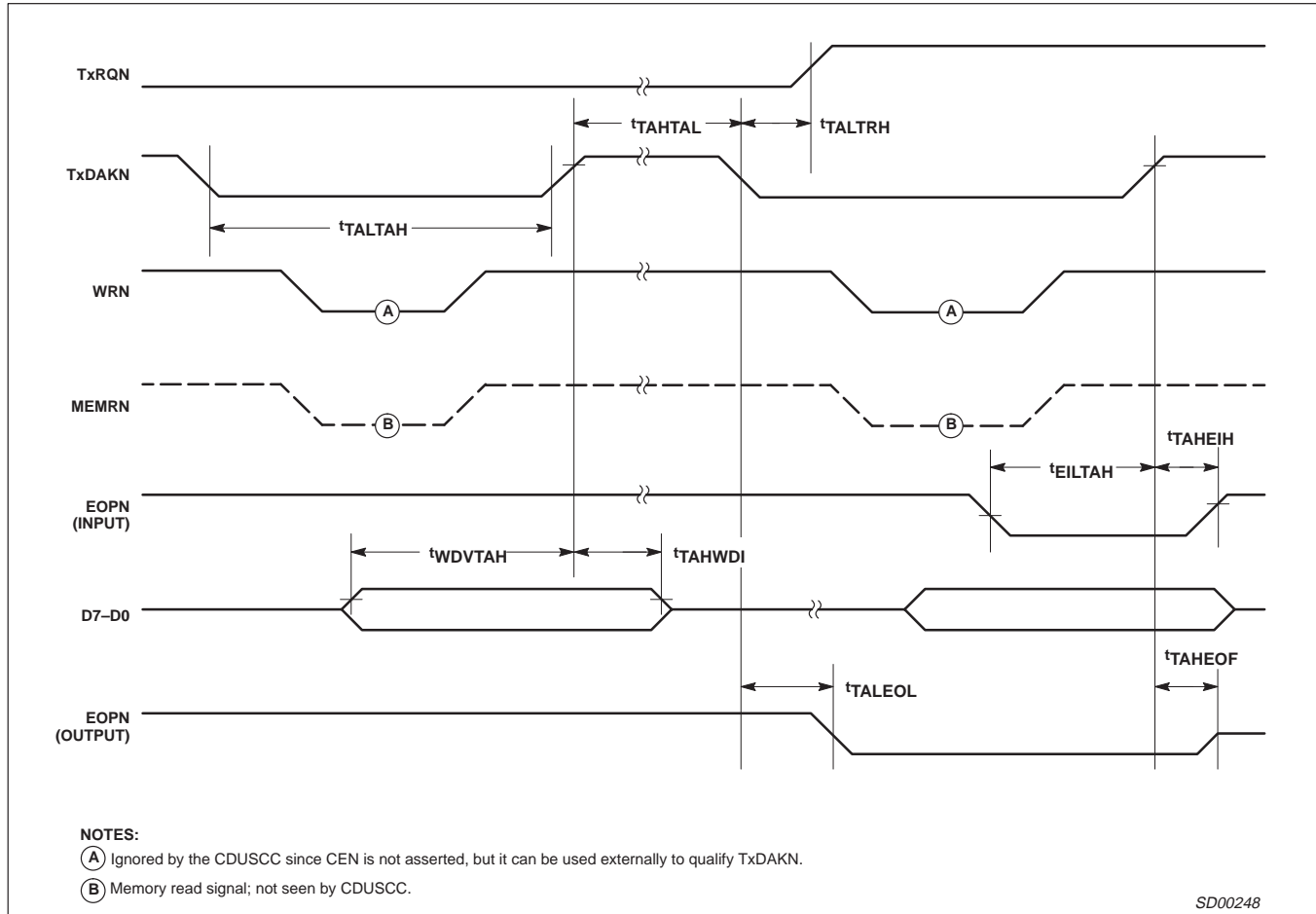


Figure 14. DMA-Transmit Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
tTAHTAL	Transmit DMA ACKN high to low time	40		30		ns
tTALTAH	Transmit DMA ACKN low to high time	110		100		ns
tTALTRH	Tx DMA ACKN low to Tx DMA REQN high					ns
tWDVTAH	Write data valid to Tx DMA ACKN high	60	110	40	100	ns
tTAHWDI	Tx DMA ACKN high to write data invalid	15		10		ns
tTALEOL	Tx DMA ACKN low to EOPN output low					ns
tTAHEOF	Tx DMA ACKN high to EOPN output float		100		80	ns
tEILTAH	EOPN input low to Tx DMA ACKN high	40	70	30	60	ns
tTAHEIH	Tx DMA ACKN high to EOPN input high	30		25		ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

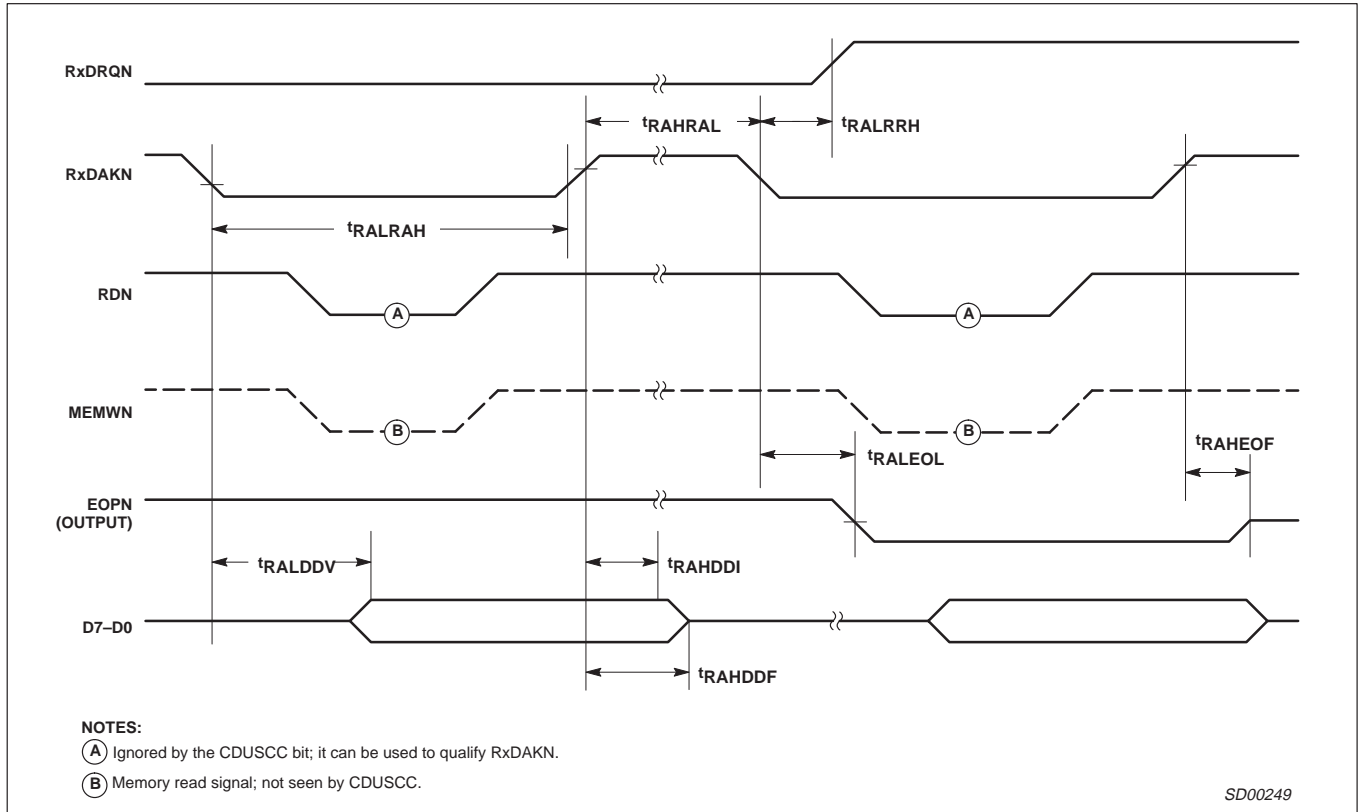


Figure 15. DMA-Receive Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
tRAHRAL	Receive DMA ACKN high to low time	50		30		ns
tRALRAH	Receive DMA ACKN low to high time	140		130		ns
tRALRRH	Rx DMA ACKN low to Rx DMA REQN high		100		100	ns
tRALEOL	Rx DMA ACKN low to EOPN output low		100		100	ns
tRAHEOF	Rx DMA ACKN high to EOPN output float		70		60	ns
tRALDDV	Rx DMA ACKN low to read data valid		140		130	ns
tRAHDDI	Rx DMA ACKN high to read data invalid	5		5		ns
tRAHDDF	Rx DMA ACKN high to data bus float		60		60	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

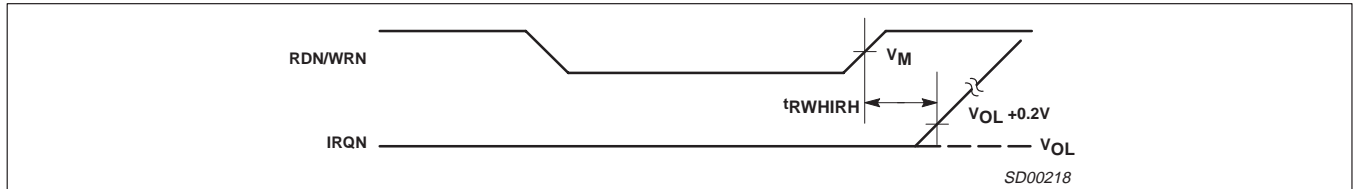


Figure 16. Interrupt Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		INDUSTRIAL SC26C562		COMMERCIAL SC26C562		
SYMBOL	PARAMETER	Min	Max	Min	Max	UNIT
t_{RWHIRH}	RDN/WRN high to IRQN high for:					
	Read Rx FIFO (RxRDY interrupt)		100		90	ns
	Write Tx FIFO (TxRDY interrupt)		100		90	ns
	Write RSR (Rx condition interrupt)		100		90	ns
	Write TRSR (Rx/Tx interrupt)		100		90	ns
	Write ICTSR (counter/timer interrupt)		100		90	ns
	Write TRMSR (Tx Path, Patt. Det.)		100		90	ns

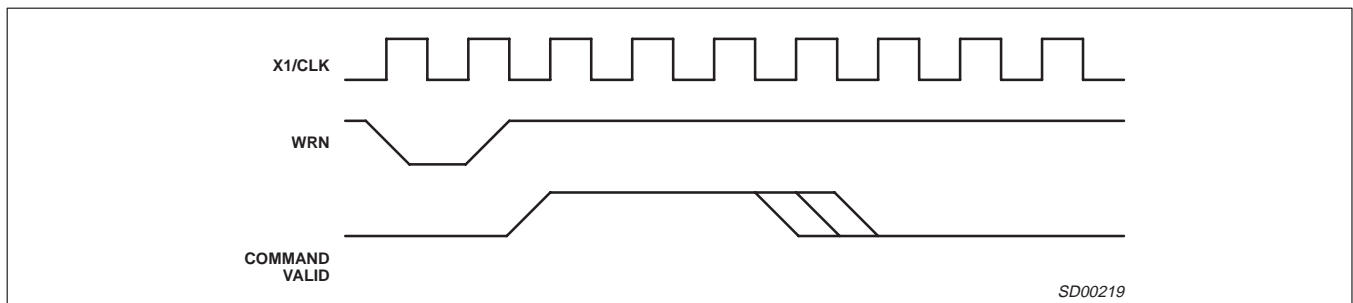


Figure 17. Command Timing

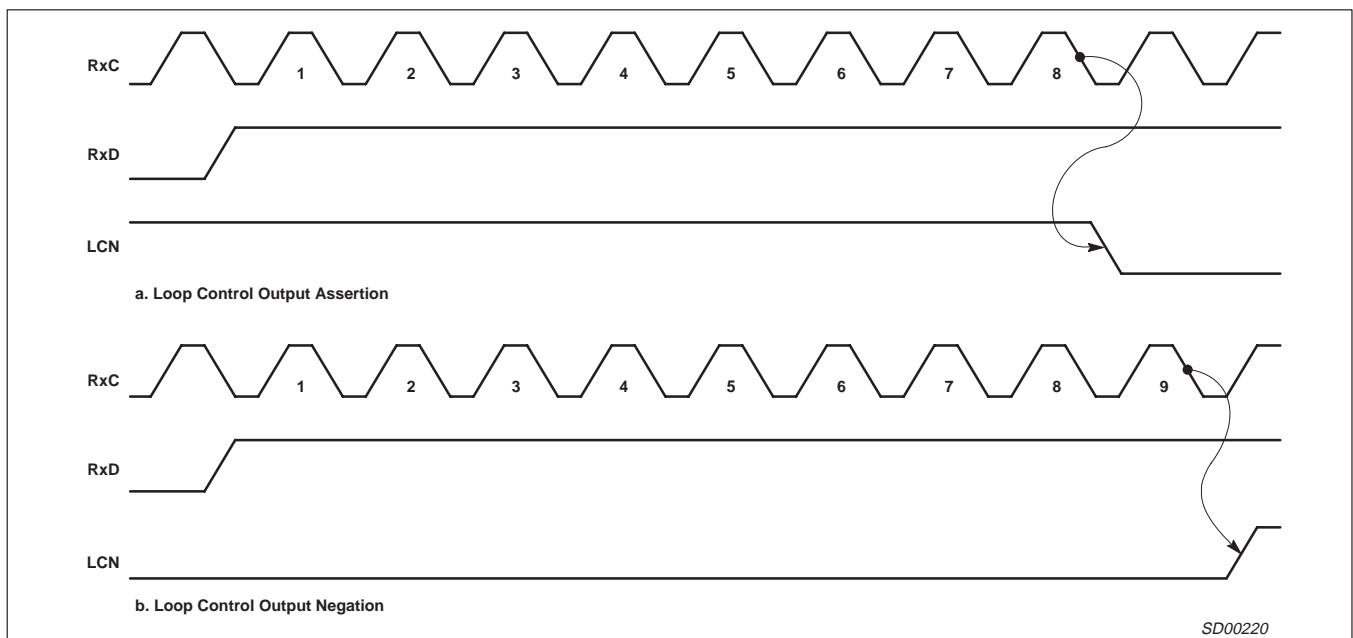


Figure 18. Relationship Between Received Data and the Loop Control Output

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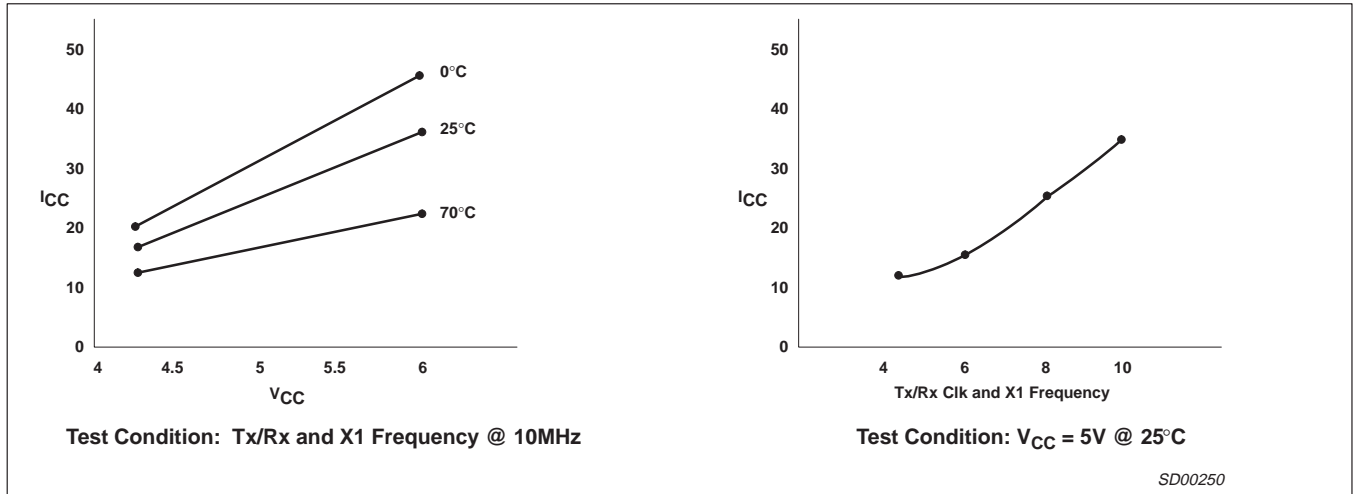


Figure 19.

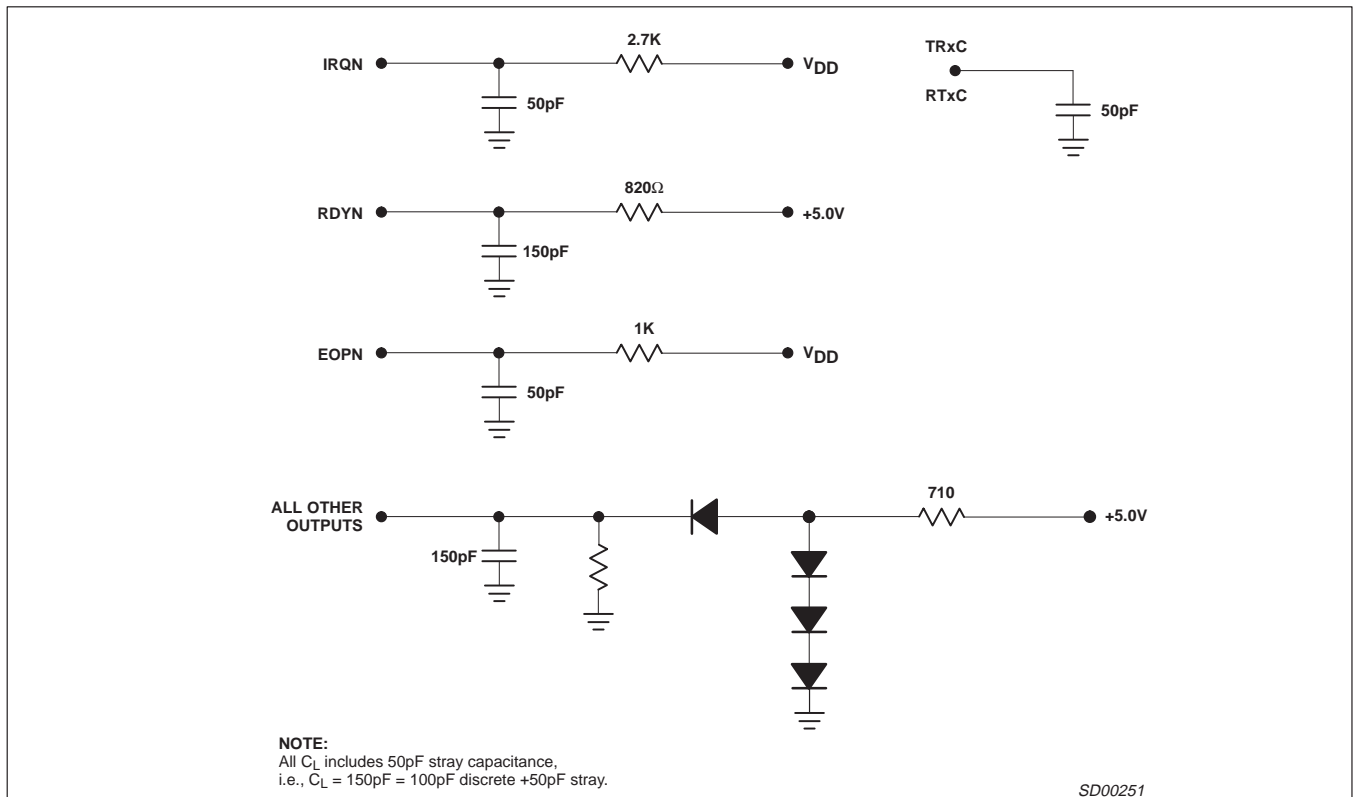


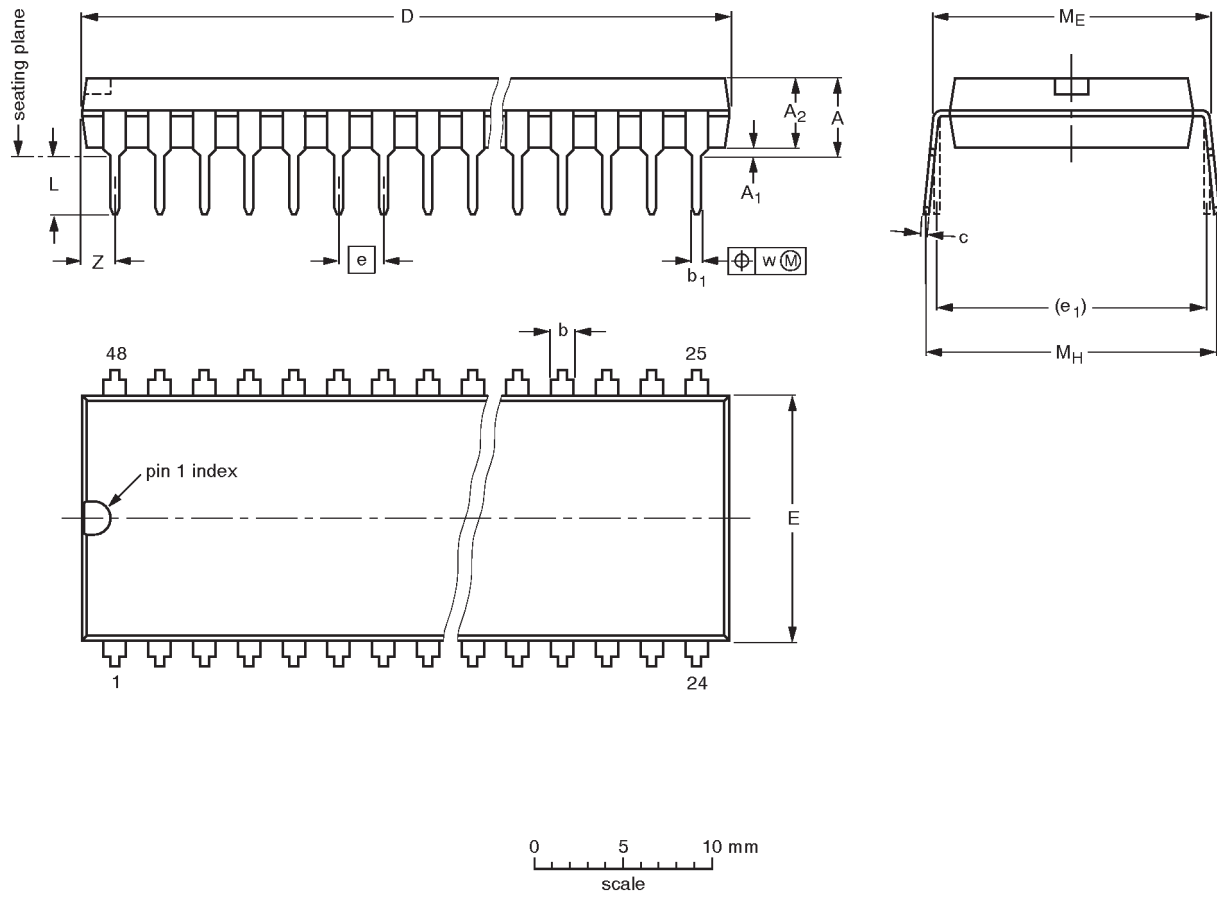
Figure 20. Test Conditions for Outputs

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DIP48: plastic dual in-line package; 48 leads (600 mil)

SOT240-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.9	0.36	4.06	1.4 1.14	0.53 0.38	0.36 0.23	62.60 61.60	14.22 13.56	2.54	15.24	3.90 3.05	15.88 15.24	18.46 15.24	0.254	2.1
inches	0.19	0.014	0.16	0.055 0.045	0.021 0.015	0.014 0.009	2.46 2.42	0.56 0.53	0.10	0.60	0.15 0.12	0.63 0.60	0.73 0.60	0.01	0.083

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

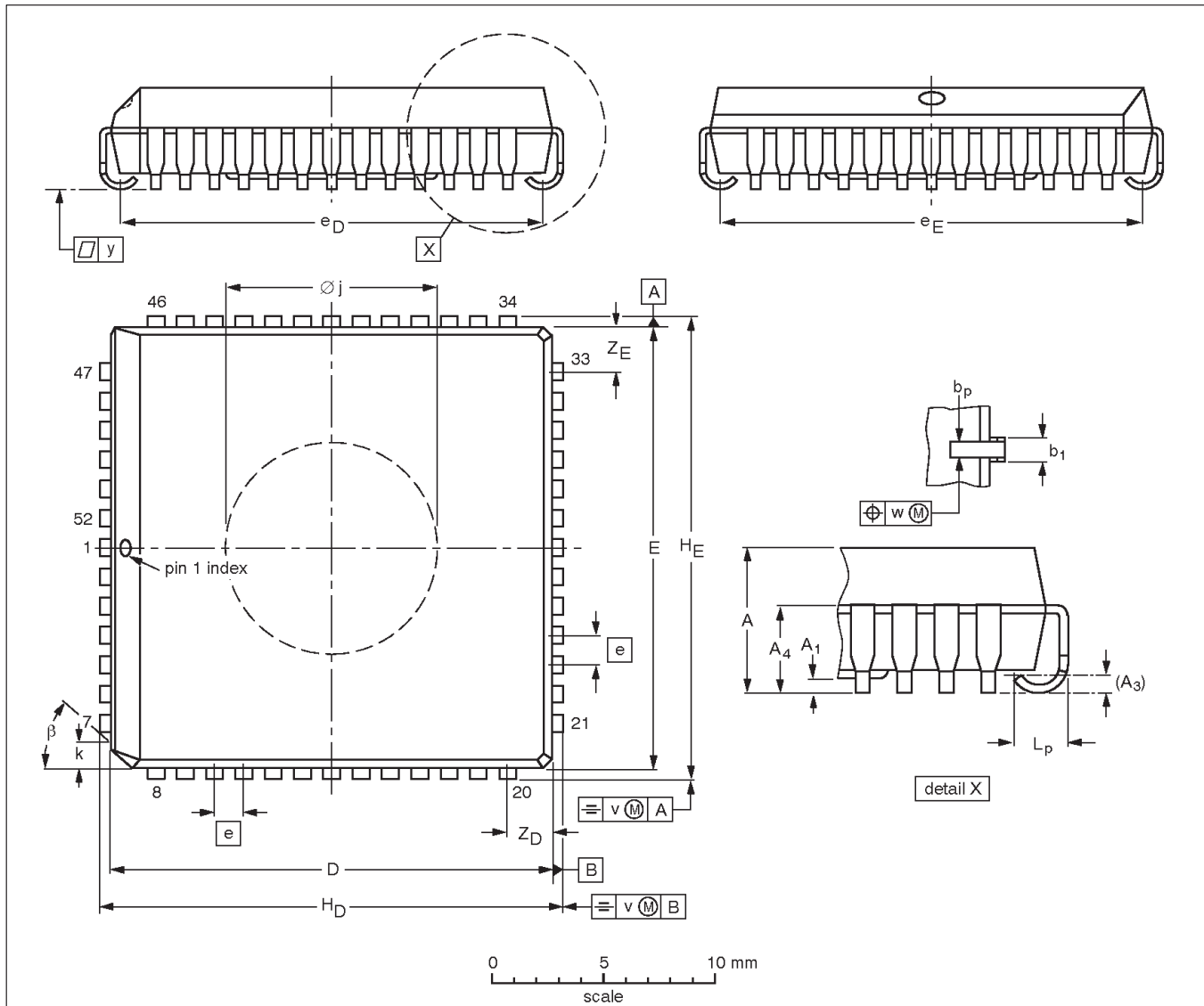
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT240-1						-92-11-17 95-01-25

CMOS dual universal serial communications controller (CSUSCC)

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PLCC52: plastic leaded chip carrier; 52 leads; pedestal

SOT238-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	∅ _j	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	19.20 19.05	19.20 19.05	1.27	18.54 17.53	18.54 17.53	20.19 19.94	20.19 19.94	1.22 1.07	9.25 9.09	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.756 0.750	0.756 0.750	0.05	0.730 0.690	0.730 0.690	0.795 0.785	0.795 0.785	0.048 0.042	0.364 0.358	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT238-3		MO-047AD			95-02-25- 97-12-16

CMOS dual universal serial communications controller (CSUSCC)

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Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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